**Amendments to the Specification:**

Please amend the paragraph beginning at line 6 of page 7 and ending at line 6 of page 7 as follows:

FIGURES ~~9-12~~ 9A-12E illustrate plots which relate to BZFLASH simulations.

Please amend the paragraph beginning at line 1 of page 16 and ending at line 7 of page 16 as follows:

FIGURES ~~9-12~~ 9A-12E illustrate plots which relate to BZFLASH simulations. Specifically, ~~FIGURE 9 contains~~ FIGURES 9A and 9B contain two output plots from a BZFLASH simulation wherein BZFLASH codes were connected to BZREFN and BZREFP cells. The supply voltage (VDDIO = S18) was swept from 1.62V to 1.98V in 0.1V increments. ~~The top plot in FIGURE 9~~ FIGURE 9A shows the decimal N- and P-code (decn and decp) versus VDDIO, and ~~the bottom plot~~ FIGURE 9B shows that the BZREFN and BZREFP outputs (zn and zp) remain below the VREF voltage (VDDIO/2) as intended.

Please amend the paragraph beginning at line 8 of page 16 and ending at line 17 of page 16 as follows:

~~FIGURE 10 contains~~ FIGURES 10A-10C contain three output plots from a BZFLASH simulation wherein BZFLASH codes were connected to BZREFN, BZREFP, and two controlled impedance buffers, BZ50T. Dither was swept from -31 to +31 by 1. ~~The top plot of~~ FIGURE 10A shows the dithered BZFLASH codes (decn and decp) and the un-dithered raw codes (fdecn and fdecp) versus dither. ~~The middle plot~~ FIGURE 10B shows the BZREFN and BZREFP

outputs (ZIN and ZIP) along with the reference VREF versus dither. ~~The bottom plot~~ FIGURE 10C shows the BZ50T pull-down and pullup output impedances (Rnio and Rpio) versus dither. Note that Rnio and Rpio are about 50ohms at a dither of zero. Also note that a +/- 4 dither count corresponds to about a +/- 10% variation in the output impedances.

Please amend the paragraph beginning at line 1 of page 17 and ending at line 8 of page 17 as follows:

~~FIGURE 11 contains~~ FIGURES 11A-11C contain three output plots from an on-chip termination (RTT) simulation using the custom I/O buffer and BZFLASH subcircuit. ~~The top plot~~ FIGURE 11A shows the minimum (rttn) and maximum (rttf) RTT for seven process corners versus "case". "Case" refers to the mixture of temperature, voltage, on-chip poly resistor value, off-chip reference resistor value, and dither. The "case" legend plot is given in ~~FIGURE 12~~ FIGURES 12A-12E. RTT target is 41ohms +/- 12.2%. Measured minimum is 34.7ohms and maximum is 45.72ohms. ~~The middle plot~~ FIGURE 11B shows the decimal P-code (decp) variation versus "case". ~~The bottom plot~~ FIGURE 11C shows the decimal N-code (decn) variation versus "case".

Please amend the paragraph beginning at line 10 of page 17 and ending at line 14 of page 17 as follows:

~~FIGURE 12 is~~ FIGURES 12A-12E are the "case" ~~legend~~ legends referred to above in connection with ~~FIGURE 11~~ FIGURES 11A-11C. ~~FIGURE 12~~ FIGURES 12A-12E ~~contains~~ contain five plots equating TEMP, VDD, VDDIO, RNPOLY, BZREXT, and BZDITHER settings to "case" numbers. "Case" numbers equate to permutations of the min/max combinations of 5 variables plus one for the nominal condition. So there are (2^5)+1 or 33 cases.